We claim:

1. An integrated circuit structure comprising in combination:

a. a semiconductor wafer having an upper surface, the semiconductor wafer having a plurality of identical die formed therein, each of the identical die having a plurality of semiconductor devices formed therein upon the surface of the semiconductor wafer;

b. a patterned layer of interconnect metal formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die, said patterned layer of interconnect metal including connection pads for making electrical connection to circuitry external to the semiconductor wafer;

c. a patterned layer of nickel plated over each connection pad for mechanically and electrically bonding to the interconnect metal forming such connection pad;

d. a patterned layer of palladium plated over the patterned layer of nickel above each connection pad for preventing the nickel from diffusing outwardly through the palladium during subsequent heating cycles; and

e. a patterned layer of gold plated over the patterned layer of palladium above each connection pad to facilitate the joinder of such connection pad with a connection element.

2. The integrated circuit structure recited by claim 1 wherein said connection element is a gold bump.

3. The integrated circuit structure recited by claim 1 wherein said connection element is a gold wire bond.

4. The integrated circuit structure recited by claim 1 wherein said connection element is a solder bump.

5. The integrated circuit structure recited by claim 1 wherein said connection element is a nickel bump.

6. The integrated circuit structure recited by claim 1 wherein the patterned layer of nickel is plated directly on top of the patterned layer of interconnect metal at each connection pad.

7. The integrated circuit structure recited by claim 1 wherein, upon each of said die, two of said connection pads are disposed within 5 micrometers of each other.

8. The integrated circuit structure recited by claim 1 wherein said patterned layer of nickel has a thickness that lies in the range of 0.5 micrometers and 20 micrometers.

9. The integrated circuit structure recited by claim 1 wherein said patterned layer of palladium has a thickness that lies in the range of 0.1 micrometers and 5 micrometers.

10. The integrated circuit structure recited by claim 1 wherein said patterned layer of gold has a thickness that lies in the range of 0.03 micrometers and 2 micrometers.

11. The integrated circuit structure recited by claim 1 wherein said patterned layer of interconnect metal is formed of copper.

12. The integrated circuit structure recited by claim 1 wherein said patterned layer of interconnect metal is formed of aluminum.

13. A process for forming connection pads on a plurality of integrated circuit die formed in a semiconductor wafer, the semiconductor wafer having an upper surface, each of the integrated circuit die having a plurality of semiconductor devices formed therein upon the surface of the semiconductor wafer, said process including the steps of:

a. forming a patterned layer of interconnect metal upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such integrated circuit die, said patterned layer of interconnect metal including

connection pads for making electrical connection to circuitry external to the semiconductor wafer;

b. following step a., forming a patterned layer of nickel by electroless plating over each connection pad for mechanically and electrically bonding to the interconnect metal at each such connection pad;

c. following step b., forming a patterned layer of palladium by electroless plating over the patterned layer of nickel above each connection pad for preventing the nickel from diffusing outwardly through the palladium during subsequent heating cycles; and

d. following step c., forming a patterned layer of gold by electroless plating over the patterned layer of palladium above each connection pad to facilitate the joinder of such connection pad with a connection element.

14. The process recited by claim 14 including the further step of joining a gold bump to the patterned layer of gold above at least one of said connection pads.

15. The process recited by claim 14 including the further step of joining a gold wire bond to the patterned layer of gold above at least one of said connection pads.

16. The process recited by claim 14 including the further step of joining a solder bump to the patterned layer of gold above at least one of said connection pads.

17. The process recited by claim 14 including the further step of joining a nickel bump to the patterned layer of gold above at least one of said connection pads.

18. The process recited by claim 14 wherein the patterned layer of nickel is plated directly on top of the patterned layer of copper metal at each connection pad.

19. The process recited by claim 14 wherein, upon each of said integrated circuit die, at least two of the connection pads are formed within 5 micrometers of each other.

20. The process recited by claim 14 wherein said step of forming a patterned layer of nickel produces a nickel layer having a thickness that lies in the range of 0.5 micrometers and 20 micrometers.

21. The process recited by claim 14 wherein said step of forming a patterned layer of palladium produces a palladium layer having a thickness that lies in the range of 0.1 micrometers and 5 micrometers.

22. The process recited by claim 14 wherein said step of forming a patterned layer of gold produces a gold layer having a thickness that lies in the range of 0.03 micrometers and 2 micrometers.

23. The process recited by claim 14 wherein said step of forming a patterned layer of interconnect metal upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices includes the step of forming such patterned layer of interconnect metal from the metal copper.

24. The process recited by claim 14 wherein said process includes the further step of heating the semiconductor wafer following the step of forming the patterned layer of gold in order to thermal cycle the plurality of semiconductor devices formed within each such integrated circuit die.